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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,038	02/08/2001	Alan Gene Gara	YOR920000192US1	4427

7590 07/30/2004

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EXAMINER	
GHULAMALI, QUTBUDDIN	
ART UNIT	**PAPER NUMBER**
2637	4

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,038	GARA, ALAN GENE	
	Examiner	Art Unit	
	Qutub Ghulamali	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-12 and 14* is/are rejected.

7)☒ Claim(s) *5 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Application filed on 02/08/2001.

Drawings

2. The drawings filed on 04/02/2001 are acceptable subject to correction of the informalities indicated herein. The drawing Figure 2, each operational block requires detailed labels. In order to avoid abandonment of this application, correction is required in reply to the Office action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U. S. C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 6, 7, are rejected under 35 U. S. C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 6, the Claim 6 recites the limitation "the producing" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Objections

5. Claims 8, and 10 are objected to because of the following informalities:

Regarding claim 8, line 1, "processing", can be replaced by --process--, and after

"positioning", --of-- can be inserted.

Regarding claim 10, line 5, after "signal", delete "voltage", line 10, delete "," after "intermediate", and line 22, replace "ans" with --and--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-9, 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Davies et al ("Davies") (US Patent No. 5,255,287).

Consider claims 1, 6, Davies discloses a method for transmitting and receiving digital (binary) data at a first transmission node via 108, the method comprises steps of encoding a serial binary data signal as a three-level modified duobinary encoded signal for transmission, the receiver comprises means for generating (arranging) a first threshold voltage and a bias voltage, the first threshold voltage being greater than the bias voltage (reference), generating a second threshold voltage that is equal to or greater than the first threshold voltage according to a peak (high) level of the first and second three-level signals, and signal detection means, operatively coupled to receive the first and second three-level signals and the second threshold voltage, for detecting logic levels in the first and second three-level signals relative to the second threshold voltage, a circuit 402 including a differential amplifier 412 having a non-inverting input terminal

connected to tap point 408, and an inverting input terminal connected to an internal bias reference voltage V.sub.BB, and for forming a serial binary signal having the detected logic levels (figs. 3A-I, 7A-C) (see col. 2, lines 50-67; col. 3, lines 1-2; col. 8, lines 11-17).

Regarding claims 7, 8, 9, 10, Davies discloses (figs. 6, 7A-C, 8) arranging binary data in serial binary bits, passing each bit in relation to first, second and third voltage levels generating (arranging) a first threshold voltage and a bias voltage, the first threshold voltage being greater than the bias voltage (reference), generating a second threshold voltage that is equal to or greater than the first threshold voltage according to a peak (high) level of the first and second three-level signals, and signal detection means, operatively coupled to receive the first and second three-level signals and the second threshold voltage, for detecting logic levels in the first and second three-level signals relative to the second threshold voltage, a circuit 402 including differential amplifier 412 having a non-inverting input terminal connected to tap point 408, and an inverting input terminal connected to an internal bias reference voltage V.sub.BB, and for forming a serial binary signal having the detected logic levels, the newly computed value applied to the data input terminal of each flip-flop circuit of PAL 502 is provided on the output at next clock tick (edge) signal clk-D1 position within a burst (frequency domain) which PAL is connected to receive, the line driver circuit 504 generates line driving signals V1, V2, V3, and V4 as new signals (col. 15, lines 47-49), (figs. 3A-I, 5, 7A-C) (see col. 2, lines 50-67; col. 3, lines 1-2; col. 8, lines 11-17; col. 15, lines 35-40).

Regarding claims 2, 4, Davies discloses binary information in serial relation to first, second and third voltage level driver amplifiers 504 (508, 510) (col. 12, lines 6-29).

Regarding claim 3, Davies discloses (fig. 2) two parallel amplifiers 212 and other part of 204 (col. 5, lines 7-27).

Regarding claim 10, 11, 12, Davies further discloses in combination with other claim limitations, binary reconstruction (synchronization) means for encoding the binary data signal for retiming the binary data signal (delay) to position output signal with respect to a clock signal responsive to output signal from amplifiers (col. 18, lines 10-14).

Allowable Subject Matter

8. Claims 5, 13, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Furuta (US Patent 4,096,526), Baker(US Patent 5,946,355) are cited as arts of reference showing binary data transmission.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (703) 305-7868. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 703 308-7728. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system.

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Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.
July 25, 2004.

7/26/04

TEMESGHEN GHEBRETINSAE
PRIMARY EXAMINER